MBI5151 Programming Guide

(This file is for controller development using and should not be shared.)

Control Command

Table 1. The control command

	Signals Combination		Description
Command Name	**LE**	**Number of DCLK Rising Edge when LE is asserted**	**Action of Command**
Stop Compulsory Error detection	High	1	Stop compulsory error detection
Data Latch	High	1	Transfer the serial data into SRAM buffer
VSYNC	High	2	Vertical Synchronal
Write Configuration 1*	High	4	Serial data are written to the configuration register 1.
Read Configuration 1	High	5	Serial data are read from the configuration register 1.
Start Compulsory Error detection	High	7	Start compulsory LED open detection
Write Configuration 2*	High	8	Serial data are written to the configuration register 2.
Read Configuration 2	High	9	Serial data are read from the configuration register 2.
Software Reset	High	10	Reset the behavior of MBI5151 except the value of configuration registers
Pre-Active	High	14	Pre-Active command needs to be sent before “Write Configuration” command.

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Definition of Configuration Register 1 and Configuration Register 2

Table 2. Configuration Register 1

MSB															LSB
F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0

e.g. Default Value

F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	1	1	0	0	6'b101011					

Bit	Attribute	Definition	Value	Function
F	Read/Write	Lower ghost elimination	0 (Default)	0: Disable
			1	1: Enabled
E	Read/Write	PWM counting mode	0(Default)	0: Forward
			1	1: Backward
D~B	Reserved	Reserved	Reserved	Reserved
A~8	Read/Write	Number of scan lines	000 001 010 011 (Default) ~ 111	000: 1 lines 001: 2 lines 010: 3 lines 011: 4 lines 100: 5 lines 101: 6 lines 110: 7 lines 111: 8 lines
7	Read/Write	Gray scale mode	0 (Default)	The 65536 GCLKs (16-bit) PWM cycle is divided into 64 sections, each section has 1024 GCLKs.
			1	The 16384 GCLKs(14-bit) PWM cycle is divided into 32 sections, each section has 512 GCLKs., User still sends 16-bit data with 2 bit 0 in LSB bits.
6	Read/Write	GCLK multiplier	0 (Default)	GCLK multiplier disable
			1	GCLK multiplier enable
5~0	Read/Write	Current gain adjustment	000000~ 111111	6'b101011 (Default) 64-steps programmable current gain, the output current can be adjusted from 12.5 % to 200%

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Table 3. Configuration Register 2

MSB															LSB
F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0

e.g. Default Value

F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
0	0	0	1	0	1	0	0	0	0	0	1	0	0	0	0

Bit	Attribute	Definition	Value	Function
F~A	Reserved	Reserved	Reserved	Reserved
9~8	Read/Write	Error detection voltage threshold	00(Default) ~11	00: 0.3V 01: 0.4V 10: 0.5V 11: 0.6V
7~4	Reserved	Reserved	Reserved	Reserved
3~1	Read/Write	Scan 0 extend	000(Default) ~111	000: 0 ns, 100: 18ns 001: 6 ns, 101: 21ns 010: 9 ns, 110: 27ns 011: 15 ns, 111: 33ns
0	Read/Write	output extend (backward valid)	0 (Default)	Disable
			1	Enabled

Recommended Settings of Configuration Register

For lower ghost elimination, the configuration register, which are shown in table 4 and 5, are recommended.

Table 4. The recommended configuration register 1 for lower ghost elimination

F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
1	0	0	0	0	1	1	1	0	0	1	0	1	0	1	1

Where, bit B-0 can be adjusted by display specification.

Table 5. The recommended configuration register 2 for lower ghost elimination

The setting of configuration register 2 for R-LED

F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
0	1	0	1	1	1	0	0	0	0	0	1	0	0	0	1

The setting of configuration register 2 for G-LED

F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
0	1	1	0	1	1	0	0	0	0	0	1	0	1	0	1

The setting of configuration register 2 for B-LED

F	E	D	C	B	A	9	8	7	6	5	4	3	2	1	0
0	1	1	1	1	1	0	0	0	0	0	1	0	1	0	1

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Initialization Sequence

At initialization, users need to program the configuration register, if the default value of the register is not what they want. Then, the users need to send the gray scale data by the number of "Data Latch" commands (16 x number of scan lines), and then send one Vsync command to start to display.

For the initial sequence, users should only send Vsync command after 50 GCLKs of the last "Data Latch" command as shown in the below waveform. The display data will not start until first Vsync command is ready. The GCLK must be stopped before Vsync command is set, and there are some timing limitations which will be described in detail in the following section.

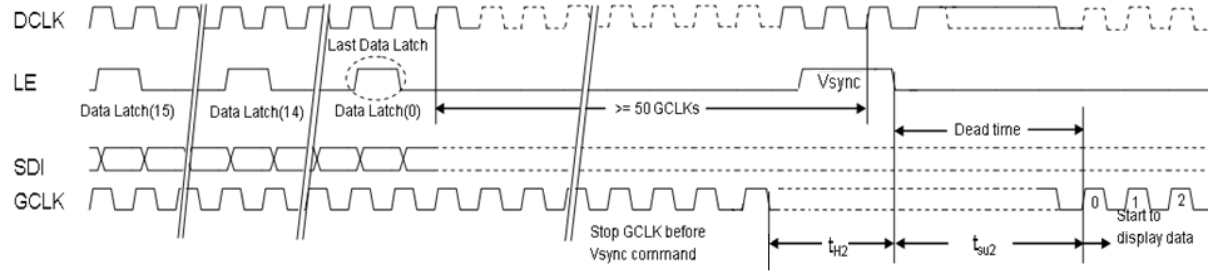

Figure 1. The timing diagram of "Data Latch" and "Vsync" command

Vsync Command Operation

Vsync command is set when users want to update the image frame. Below waveforms show the Vsync command to update the frame, when GCLK is independent or equal to DCLK.

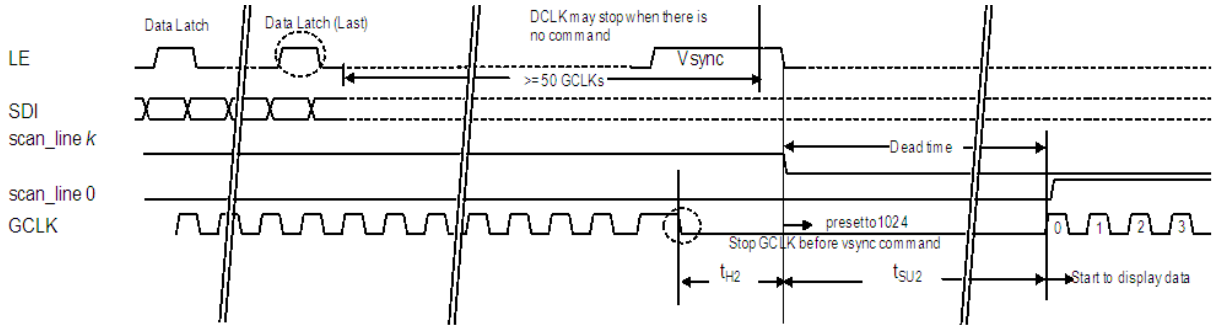

Figure 2. The timing diagram of Vsync command when update the image frame

Limitations

1. Since the gray scale data needs time to pre-read from SRAM to internal display buffer after last Data Latch command, there should be at least 50 GCLKs before the Vsync command is sent
   Note: More details about SRAM memory structure can be referred to the section of Memory Structure.
2. It is suggested for controller to keep one GCLK counter (from 0~1024), which will preset to 1024 at the falling edge of LE of Vsync command and restart from 0 at next GCLK.
3. Since Vsync is the LE clock domain, there is a timing limitation between LE and GCLK. The GCLK should stop before Vsync command is sent. The setup and hold time between LE's falling edge and GCLK's rising edge must meet the t_{SU2} and t_{H2}, respectively.
4. The GCLK also needs to stop for dead time. The dead time is the time interval between scan lines, and is controlled by stopping GCLK. When Vsync command is set, the frame will be updated. The scan line needs to be switched (by controller) from scan line *k* to scan line 0, too.
5. DCLK can either stop or not when there is no command.
6. During dead time, user needs to either stop DCLK or cannot send "Data Latch" command.
7. The new data will be loaded to internal display buffer at Vsync command. But it will start to display after dead time is finished.

Switch Scan Line Inside Each Frame

For the control of scan line switch, users should count in the same way of MBI5151's GCLK counter and switch each scan line when MBI5151 GCLK counter counts to 1023, and please refer to the section of Gray Scale Mode and Scan-type S-PWM for the multiplexing sequence. The dead time is controlled by stopping GCLK. MBI5151 will turn off output channels when GCLK counter value equals to 1024 during dead time.

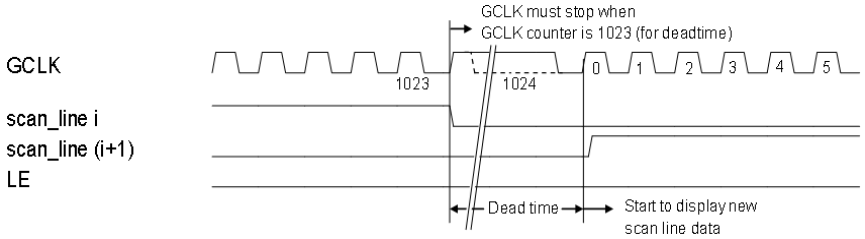

Figure 3. The sketch of scan line switched in dead time

The control sequence is described as below:

1. Users program the configuration register by "Write Configuration" command.
2. Users send gray scale data by the number of "Data Latch" commands (16 x number of scan lines).
3. After last "Data Latch" command, users must wait for more than 50 GCLKs before sending Vsync command. If it is not the first frame, users should send Vsync command according to the frame rate. For example, if the frame rate is 60, users should wait for 1/60 seconds. When users send Vsync command, the related timing limitations must be followed.

4. When users send Vsync command, the scan line needs to start to count from 0. GCLK counter needs to be pre-set to 1024 and stops GCLK for dead time.
5. During the frame display period, users need to keep one GCLK counter (0~1024) and switch scan line and insert dead time (by stopping GCLK) when GCLK counter counts to 1023.
6. During dead time (both for sending Vsync command or when GCLK counter equals to 1024), it's not allowed to send "Data Latch" command.
7. The gray scale data of the next frame may be sent after Vsync command is sent.
8. It's strongly recommend that "Write Configuration" command should be sent periodically to avoid system noise interference.

Low gray scale Compensation

In order to enhance the display uniformity in low gray scale, the recommended settings are

- For R-LED

  -cfg1[E] = 0, cfg2[0] =0, δf = 0~100ns, step: 10ns

- For G-LED

  -cfg1[E] = 1, cfg2[0] =1, δ = 0~100ns, step: 10ns

- For B-LED

  -cfg1[E] = 1, cfg2[0] =0, dh = 20~200ns, step: 10 ns or 20ns

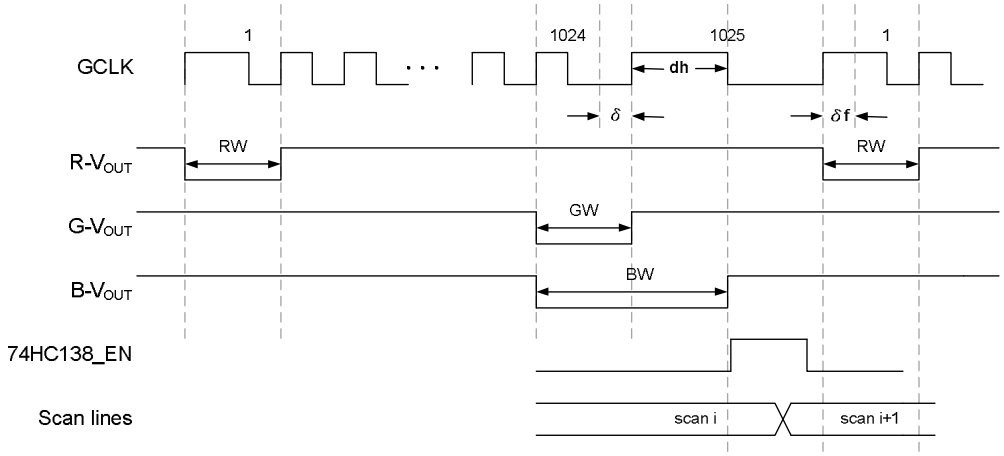

Figure 4. Controller Compensation

The varied stray capacitors in R/G/B LEDs cause the problems of white color cast and insufficient brightness at low grayscale. Therefore, the extended time of R/G/B LEDs must be set up separately. Figure 4 shows the sketch and the details are described as below

1. δf: The increased high pulse width of 1st GCLK. When PWM forward counting and the grayscale is 1, the output pulse width becomes 1/GCLK +δf.
2. δ: The increased low pulse width of 1024th GCLK. When PWM backward counting and the grayscale is 1, the output pulse width becomes 1/GCLK +δ.

3. dh: The increased high pulse width of 1025th GCLK. When PWM backward counting and the grayscale is 1, the output pulse width becomes 1/GCLK +δ+ dh.

The recommended set-up for R/G/B LEDs is

R-LED: Forward counting

G-LED: Backward counting

B-LED: Backward counting + output extend

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Visual Refresh Rate

In 16-bit S-PWM mode, the visual refresh rate will be improved by 64x, if the data is ≧64.
In 14-bit S-PWM mode, the visual refresh rate will be improved by 32x, if the data is ≧32.

The formula of visual refresh rate is:

GCLK Multiplier Disable

In 16-bit S-PWM mode, visual refresh rate = GCLK frequency / [(1024 GCLK + dead time) x number of scan lines]
In 14-bit S-PWM mode, visual refresh rate = GCLK frequency / [(512 GCLK + dead time) x number of scan lines]

For example, if there are 8 scan lines with 16-bit scan-type S-PWM, the GCLK frequency is 10MHz. The dead time is 10 GCLK periods. Then the visual refresh rate could be calculated as below:
Visual refresh rate = 10MHz / [(1024+10) x 8] = 1208Hz.

GCLK Multiplier Enable

In 16-bit S-PWM mode, visual refresh rate = GCLK frequency / [(512 GCLK + dead time) x number of scan lines]
In 14-bit S-PWM mode, visual refresh rate = GCLK frequency / [(256 GCLK + dead time) x number of scan lines]

Compulsory Error Detection

The principle of MBI5151 LED compulsory error detection is to compare the output voltage (V_{DS}) and the threshold voltage of error detection ($V_{DS,\ TH}$). The threshold voltage can be set up through the bit 9~8 in configuration register 2. When MBI5151 executes the compulsory error detection, all the output channels will be turned off temporarily. The error report will be pushed out from SDO after MBI5151 receives the command to stop compulsory error detection. The duration of compulsory error detection longer than 700ns is recommended.

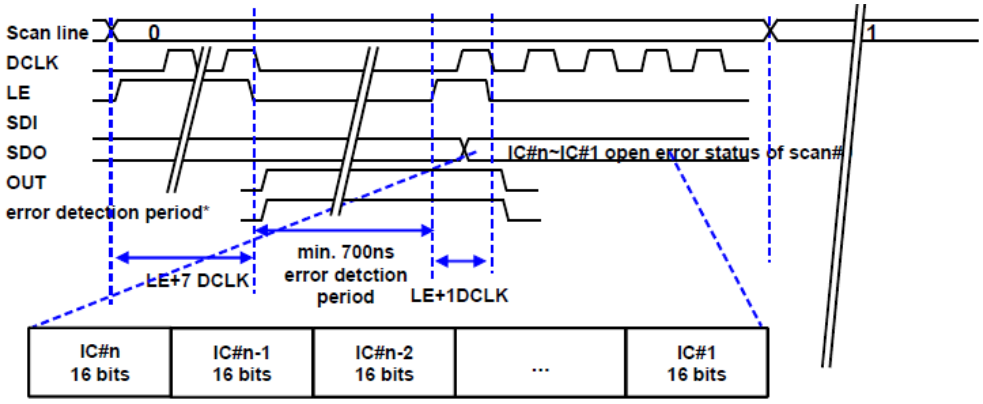

Figure 5. Compulsory Error Detection